An Efficient Inductor-less Dynamically Configured Interface Circuit for Piezoelectric Vibration Energy Harvesting

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***Abstract*—Vibration energy harvesting based on piezoelectric materials is of interest in several applications such as in powering remote distributed wireless sensor nodes for structural health monitoring. Synchronized Switch Harvesting on Inductor (SSHI) and Synchronous Electric Charge Extraction (SECE) circuits show good power efficiency among reported power management circuits; however, limitations exist due to inductors employed, adaption of response to varying excitation levels and the Synchronized Switch Damping (SSD) effect. In this paper, an inductor-less dynamically configured interface circuit is proposed, which is able to configure the connection of two piezoelectric materials in parallel or in series by periodically evaluating the ambient excitation level. The proposed circuit is designed and fabricated in a $0.35\,\mu\mathrm{m}$ HV CMOS process.The fabricated circuit is co-integrated with a piezoelectric bimorph energy harvester and the performance is experimentally validated. With a low power consumption ($0.5\,\mu\mathrm{W}$), the measured results show that the proposed rectifier can provide a 4.5 $\times$ boost in harvested energy compared to the conventional full-bridge rectifier without employing an inductor. It also shows a high power efficiency over a wide range of excitation levels and is less susceptible to SSD.**

***Index Terms*—Energy harvesting, piezoelectric transducer, rectifier, power conditioning.**

I. Introduction

ULTRA low power wireless sensors and sensor systems [1], [2] are of increasing interest in a variety of applications ranging from structural health monitoring to industrial process control [3], [4]. Compared to the wired methodologies, wireless devices provide many advantages, such as flexibility and ease of placing the sensors in locations that are not accessible by the wired counterparts. However, considerations of ultra low power are increasingly important for all wireless devices including sensors [5]. By minimizing the power consumption, researchers and engineers have attempted to extend battery lifetime and to avoid replacing or recharging batteries too frequently. While batteries have remained the primary energy sources due to their energy density, in certain sensing contexts requiring the operation of sensors and sensor systems over a significant period of time [6], including implantable biomedical electronic devices [7] and tire pressure sensors [8], battery usage may be both impractical and add extra cost due to the requirements for periodic re-charging and/or replacement [9]. In order to address this challenge and extend the operational lifetime of wireless sensors, there has been an emerging research interest to harvest energy from environmental kinetic vibration [10], [11].

Among all vibration energy harvesters (VEH), piezoelectric materials are widely used due to their scalability and compatibility with integrated circuit technologies [12] compared to their electrostatic [13] and electromagnetic counterparts [14]. The piezoelectric transducer (PT) has to be designed to not only produce as much raw power as possible, but the interface circuit also needs to be able to extract most of power from the PT with very low power consumption. Full-bridge rectifiers are widely used in commercial energy harvesting systems due to their simplicity and stability; however, they set high threshold voltages for the generated energy to be extracted by the circuit. While vibrating at or close to its resonance, a PT can be modeled as a current source I_P connected in parallel with a plate capacitor C_P and a resistor R_P. Fig. 1 shows the full-bridge rectifier connected with a PT and the associated waveforms. In order to transfer the generated energy from the PT to the storage capacitor C_S, the voltage across the PT V_{piezo} should attain $V_S + 2V_D$ or $-(V_S + 2V_D)$. Hence the energy used to charge the internal capacitor C_P from V_S+2V_D to $-(V_S + 2V_D)$ (or vice-versa) is wasted.

In order to increase the power efficiency of a VEH system, most of active rectifiers seek to develop a mechanism to minimize the energy wasted in charging C_P. An SSHI (Synchronized Switch Harvesting on Inductor) rectifier was presented in [15] to employ an inductor to flip the voltage V_{piezo} at zero-crossing points of I_P. Chip and board level measurements of SSHI rectifiers have been previously implemented in [16], [17] to demonstrate their high power efficiency. Other synchronized switch interfaces, such as Synchronous Electric Charge Extraction (SECE), are also widely used for high-efficiency circuits [18].

Although SSHI and SECE rectifiers can transfer most of charge to a storage capacitor at specific conditions, they have a few main drawbacks that need to be mentioned. First, SSHI and SECE circuits require inductors, which must be implemented off-chip to achieve good performance and such an inductor can be the main factor in increasing the overall volume of the energy harvesting system. In addition, SSHI circuits can only achieve high efficiency at a limited range of excitation levels. This limits the overall performance of the circuit in real-world implementations, where the excitation level varies with time unpredictably in a wide range. Although this is not an issue for an SECE circuit due to its different ar-

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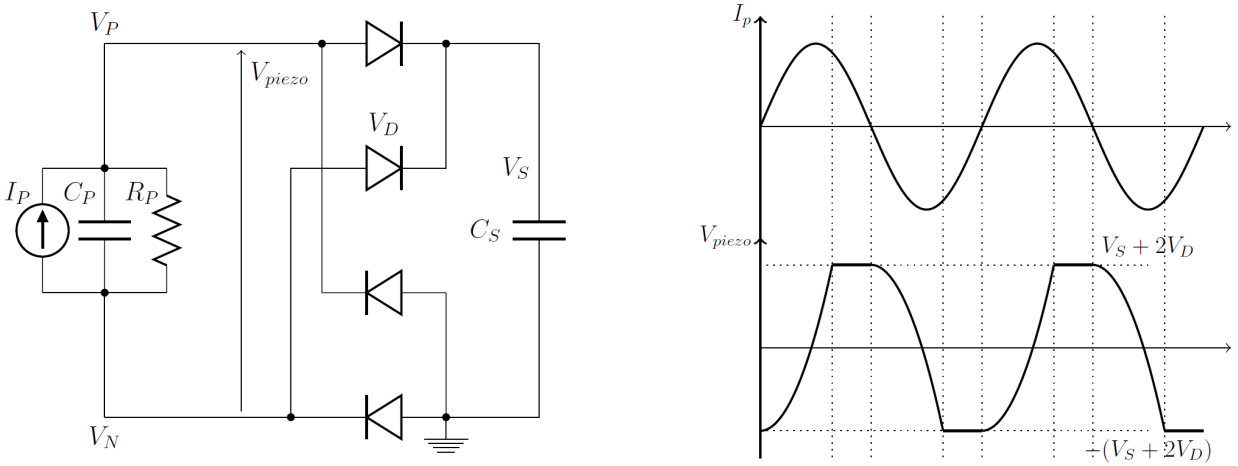


(a) Full-bridge rectifier

(b) I_p and V_{piezo} waveform

Fig. 1: Full-bridge rectifier for piezoelectric VEH and the associated waveforms

chitecture to extract energy, it required more complex circuits to be implemented compared to other circuits. Furthermore, SSHI and SECE can only provide higher performance than simple full-bridge rectifiers for weakly coupled piezoelectric transducers due to the synchronized switch damping effect. If the the coupling is strong and the PT vibrates at resonance, the periodic current pulses applied to invert (for SSHI) or extract (for SECE) charge on a PT result in an electrical actuation that opposes the vibration, which is known as Synchronized Switch Damping (SSD) [19], [20]. Due to the relatively strong nonlinear damping introduced, this principle has also been used for wave reflection/transmission reduction [21], where an architecture similar to SSHI was used to perform the charge inversion to increase the electrical actuation. This negative force feedback is basically introduced by the first harmonic of the current pulses. If the current pulses are lower and wider (lower amplitude and lower first harmonic frequency), the SSD becomes less significant and synchronized switch circuits can thus transfer charge. All of the above limitations introduced by inductors, real-world wide range excitation levels and SSD effect result in the SSHI and SECE rectifiers achieving acceptable performance only in a limited operating range.

This paper proposes a fully integrated CMOS interface circuit interfaced to a bimorph PT to automatically switch the connection of the two PTs to increase output power based on the amplitude of the input excitation, thereby enabling a significant improvement in power extraction efficiency for the immediate electrical interface. With the proposed circuit, the two PTs are connected in parallel or in series according to the environmental excitation level by periodically evaluating the excitation amplitude. As compared to the SSHI or SECE rectifiers, the proposed circuit does not employ any inductor, which significantly decrease the expected overall volume of the system, especially for MEMS low-volume energy harvesters. In addition, dynamically switching between parallel and series configurations allows the energy harvester to achieve a high power efficiency over a wide range of input excitation amplitudes. In terms of the SSD problems for SSHI and SECE rectifiers, the proposed circuit enables shifting between different configurations instead of performing synchronized charge inversion or extraction. Hence it avoids introducing negative force feedback and it is less subject to the SSD introduced by the circuit, which extends the range over which the circuit can operate efficiently.

This paper consists of six sections presenting the proposed circuit covering modeling and experimental validation. In the next section, parallel and series connections of two PTs are theoretically studied to identify the conditions when one configuration is working better than the other one. Identifying the switching condition between parallel and series models is very important to implement the associated algorithms in designing the circuit. The third section gives an overall description of the proposed interface circuit and the fourth section provides details in circuit implementations of each functional block of the system. The fabricated chip is experimentally evaluated in the fifth section and the final section provides a summary and conclusion.

II. Modeling of Parallel and Series Configurations

In this section, theoretical models are developed to compare the performance between parallel and series connections of a bimorph cantilever. In order to compare the performance, there are two methods to evaluate the output power from the both models. One way is to change excitation amplitude (corresponding to voltage V_{piezo}) with a fixed V_S; another way is to change the voltage V_S for a fixed excitation amplitude. The proposed rectifier aims to choose an appropriate connection type according to both excitation amplitude and V_S value to maximize output power.

A. Parallel model

As the two piezoelectric transducers (PT) are located on the both sides of a single bimorph cantilever, they have exactly the same frequencies, amplitudes and phases. While the two PTs are connected in parallel, the parallel model can be considered

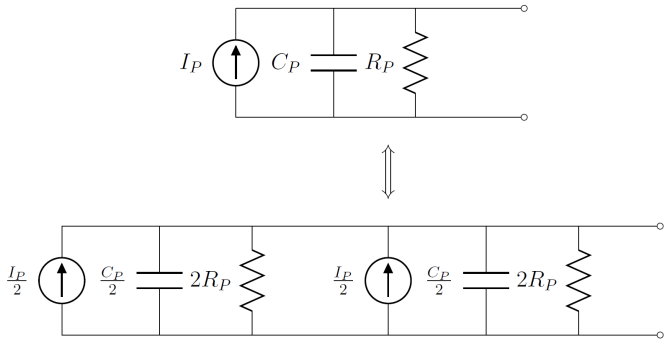


Fig. 2: A monolithic PT (top) and two PTs connected in parallel (bottom)

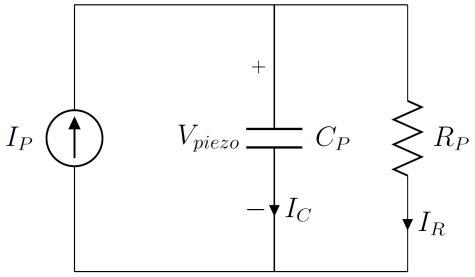


Fig. 3: Current flow in a piezoelectric generator

as a $2\times$ larger monolithic PT with frequency, amplitude and phase unchanged, see Fig. 2. Assuming the excitation is sinusoidal, the current source, capacitor and resistor for the resulting parallel model can be written as $I_P = I_0 \sin 2\pi f_P t$, C_P and R_P. Hence, the corresponding parameters for one single PT are $\frac{1}{2}I_P$, $\frac{1}{2}C_P$ and $2R_P$. For the parallel model, the total generated charge in a half cycle T/2 should first be calculated and can be written as:

$$Q_{total} = \int_0^{\frac{T}{2}} I_0 \sin \omega t \mathrm{d}t = \frac{2I_0}{\omega} \tag{1}$$

Before the full-bridge rectifier becomes conducting, the current from I_P is split into two parts inside the piezoelectric harvester, I_C and I_R flowing through the capacitor and resistor respectively (see Fig. 3). As the rectifier is not yet conducting in this case, the PT can be regarded as operating in an open-circuit. Hence, the charge flowing into the capacitor C_P can be written as:

$$Q_C(j\omega) = Q_{total}\frac{I_C}{I_P}(j\omega) = \frac{2jI_0R_PC_P}{1+j\omega R_PC_P} \tag{2}$$

Besides the charge flowing into C_P to form the voltage V_{piezo}, the rest of the charge is dissipated by the resistor R_P. According to the formula $V = Q/C$, the open-circuit peak-to-peak voltage $V_{pp(open)}$ is expressed as:

$$\begin{aligned} V_{pp(open)} &= |\frac{Q_C(j\omega)}{C_P}| = |\frac{2jI_0R_P}{1+j\omega R_PC_P}| \\ &= \frac{2I_0R_P}{\sqrt{1+\omega^2R_P^2C_P^2}} \end{aligned} \tag{3}$$

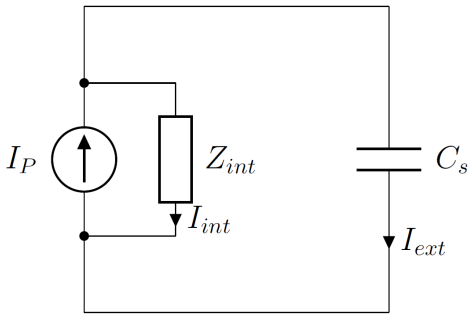


Fig. 4: Current flow while charging C_s - parallel model

In order to be able to charge the capacitor C_S, the voltage $V_{pp(open)}$ should be greater than the threshold $V_{TH} = 2(V_S + 2V_D)$. Hence, the condition for the rectifier to start transferring charge from the PT to C_S is:

$$\begin{aligned} &V_{pp(open)} > 2(V_S + 2V_D) \\ \Rightarrow &\frac{I_0R_P}{\sqrt{1+\omega^2R_P^2C_P^2}} > V_S + 2V_D \end{aligned} \tag{4}$$

Assuming $V_S = 2\,\mathrm{V}$ and $V_D = 0.3\,\mathrm{V}$, the condition for commencing transferring energy for the parallel model is $V_{pp(open)} > 2(V_S + 2V_D) = 5.2\,\mathrm{V}$. In order to compare the performance between parallel and series models, this condition is assumed to be always satisfied. The charge flowing into C_P is expressed in (2). After a part of charge is wasted for charging C_P, V_{piezo} equals to $V_S + 2V_D$ (or $-(V_S + 2V_D)$) and the rectifier becomes conducting. The wasted charge can be expressed as: $Q_{wasted} = 2C_P(V_S + 2V_D)$. Therefore, the charge going through the rectifier is the difference between Q_C and Q_{wasted}:

$$\begin{aligned} Q_{remain}(j\omega) &= Q_C(j\omega) - Q_{wasted} \\ &= 2C_P(\frac{jI_0R_P}{1+j\omega R_PC_P} - (V_S + 2V_D)) \end{aligned} \tag{5}$$

After the rectifier becomes conducting, the voltage V_{piezo} attains the threshold and the equivalent circuit transforms to a harvester in parallel with C_S as shown in Fig. 4. The internal impedance of the piezoelectric harvester is the value that C_P and R_P in parallel, expressed as $Z_{int}(j\omega) = \frac{1}{j\omega C_P}//R_P = \frac{R_P}{1+j\omega R_PC_P}$. Hence, the charge flowing into C_S can be written as:

$$\begin{aligned} Q_S(j\omega) &= Q_{remain}\frac{Z_{int}}{Z_{int} + \frac{1}{j\omega C_S}} \\ &= \frac{2j\omega R_PC_PC_S}{1+j\omega R_P(C_P+C_S)}(\frac{jI_0R_P}{1+j\omega R_PC_P} - (V_S + 2V_D)) \end{aligned} \tag{6}$$

The capacitor C_S at the output of the rectifier is usually chosen at a value much higher than the PT internal capacitor C_P ($C_S \gg C_P$), so that V_S can keep increasing steadily. In addition, as R_P is usually between hundreds of $\mathrm{k}\Omega$ and several $\mathrm{M}\Omega$, hence $\omega R_PC_S \gg 1$. Therefore, (6) can be approximately written as:

$$\begin{aligned} Q_S &\approx 2C_P(\frac{I_0 R_P}{\sqrt{1+\omega^2 R_P^2 C_P^2}} - (V_S + 2V_D)) \\ &= 2C_P(\frac{V_{pp(open)}}{2} - (V_S + 2V_D) \end{aligned} \tag{7}$$

So that the voltage increase in C_S for the parallel model in a half I_P cycle is expressed as (where the subscript "//" means "parallel"):

$$\Delta V_{S//} = \frac{Q_S}{C_S} = \frac{C_P}{C_S}(V_{pp(open)} - 2(V_S + 2V_D)) \tag{8}$$

B. Series model

For the two PTs connected in series, the calculation starts with considering a single harvester, for which the internal current flow is similar to that shown in figure 4 and V_{piezo1} is the voltage generated by one single source. As there are two PTs connected in series, the total voltage is $V_{piezo} = \sum_{i=1}^{2} V_{piezo_i} = 2V_{piezo1}$. As the condition to charge C_S is $V_{piezo} > 2(V_S+2V_D)$, hence this condition for each individual source is $V_{piezo1} > V_S+2V_D$. It can be seen that the threshold voltage is now lowered by two times compared to the parallel model so that harvester is more likely to start operating at lower excitation levels. Hence, the charge flowing into C_{P1} in a half cycle is:

$$Q_{\frac{T}{2}1}(j\omega) = \int_0^{\frac{T}{2}} I_{p1} \frac{R_{P1}}{R_{P1} + \frac{1}{j\omega C_{p1}}} = \frac{I_0 R_P C_P}{1 + j\omega R_P C_P} \tag{9}$$

The wasted charge for dis-charging and charging in one source in a half cycle is:

$$Q_{wasted1} = C_{p1}(V_S + 2V_D) = \frac{C_p}{2}(V_S + 2V_D) \tag{10}$$

Before the condition $V_{piezo1} > V_S + 2V_D$ is met, the harvester is disconnected from C_S (as the diodes in the rectifier are not conducting). Once the $V_{piezo1} > V_S+2V_D$ is satisfied, all of the sources are connected together with C_S in series. At this time, C_S starts to be charged and the remaining charge for each single source that can be used for charging is:

$$\begin{aligned} Q_{remain1}(j\omega) &= Q_{\frac{T}{2}1}(j\omega) - Q_{wasted1} \\ &= C_P(\frac{I_0 R_P}{1 + j\omega R_P C_P} - \frac{V_S + 2V_D}{2}) \end{aligned} \tag{11}$$

As only one harvester is considered, superposition theory can be used to turn off the current source of the other harvester. While the rectifier is conducting, the equivalent circuit for one single source is shown in figure 5. As the total internal capacitance and resistance for the parallel model are C_P and R_P, these values for one single PT becomes $C_P/2$ and $2R_P$. Hence, the internal impedance for one PT is $Z_{int1}(j\omega) = \frac{2}{j\omega C_P} // 2R_P = \frac{2R_P}{1+j\omega R_P C_P}$. Therefore, the ratio between the I_{ext} and I_{int} for each source being studied is:

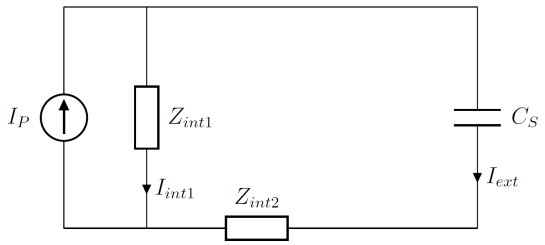


Fig. 5: Equivalent circuit for two PTs connected in series for charging C_S

$$\begin{aligned} &\frac{I_{ext}}{I_{int}} = |\frac{Z_{int1}}{Z_{int1} + Z_{int2} + \frac{1}{j\omega C_S}}| \approx \frac{1}{2} \\ &(\text{as} \quad C_S \gg C_P \quad \text{and} \quad Z_{int1} = Z_{int2}) \end{aligned} \tag{12}$$

Therefore, the total charge that flows into C_S from one single source is:

$$Q_{S1} = |\frac{1}{2} Q_{left1}(j\omega)| = \frac{C_P}{2}(\frac{I_0 R_P}{\sqrt{1+\omega^2 R_P^2 C_P^2}} - \frac{V_S + 2V_D}{2}) \tag{13}$$

With consideration of the other PT, the total charge that flows into C_S is (the subscript "+" in the expression represents series connection):

$$Q_{S+} = 2Q_{S1} = C_P(\frac{I_0 R_P}{\sqrt{1+\omega^2 R_P^2 C_P^2}} - \frac{V_S + 2V_D}{2}) \tag{14}$$

The voltage increase in C_S is:

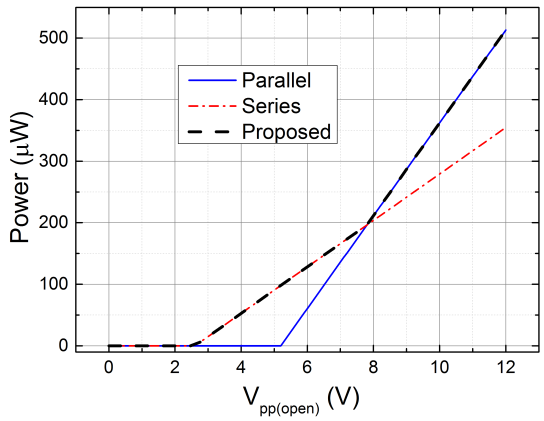
$$\Delta V_{S+} = \frac{Q_{S+}}{C_S} = \frac{C_P}{C_S}(\frac{V_{pp(open)}}{2} - \frac{V_S + 2V_D}{2}) \tag{15}$$

C. Performance comparison and proposed scheme

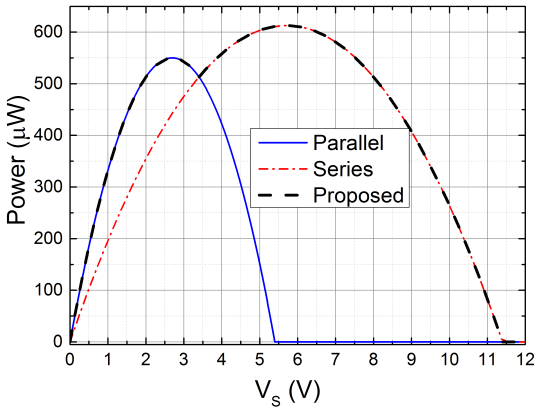
The voltage increase values in V_S for both parallel and series models are expressed in (8) and (15). As these are the voltage variation in a half I_P period, the output power for both models can be calculated by dividing the increased energy stored in C_S by the half period:

$$P = \frac{\frac{1}{2} C_S((V_S + \Delta V_S)^2 - V_S^2)}{T/2} = f_P C_S((V_S + \Delta V_S)^2 - V_S^2) \tag{16}$$

where ΔV_S can be either $\Delta V_{S//}$ expressed in (8) for the parallel model or ΔV_{S+} expressed in (15) for the series model. With given diodes (fixed V_D), there are two variables in (16): $V_{pp(open)}$ and V_S. The performance of both models can be compared while fixing one of these variables and varying the other one. Fig. 6 shows the theoretical comparison of parallel and series models in function of excitation amplitude (Fig. 6a) and in function of V_S (Fig. 6b), where the diode voltage drop is set as $V_D = 0.3\,\text{V}$. It can be seen that each model has an optimal operation range compared to the other model. Hence, it is useful to find the condition when the parallel model



(a) Output power in function of excitation level with fixed $V_S = 2\,\mathrm{V}$



(b) Output power in function of V_S with fixed excitation level of $V_{pp(open)} = 12\,\mathrm{V}$ (acceleration: 8.0 g)

Fig. 6: Theoretical output power for parallel model, series model and proposed model (diode voltage drop set as $V_D = 0.3\,\mathrm{V}$)

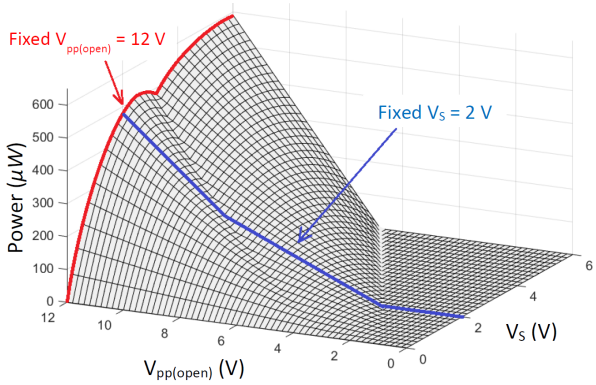


Fig. 7: 3-D surface plot of theoretical output power in function of $V_{pp(open)}$ and V_S

outputs higher power than the series model. This condition can be found by setting $\Delta V_{S//} > \Delta V_{S+}$:

$$\frac{C_P}{C_S}(V_{pp(open)} - 2(V_S + 2V_D) > \frac{C_P}{C_S}(\frac{V_{pp(open)}}{2} - \frac{V_S + 2V_D}{2}) \Rightarrow V_{pp(open)} > 3(V_S + 2V_D) \tag{17}$$

It should be noticed that the value $V_{pp(open)}$ is the voltage while the two PTs are connected in parallel because this value doubles for the series model. The inequality in (17) shows the condition that the parallel model can generate more output power than the series model. Fig. 6 shows that the output power difference from the two models can be significant in some cases. Therefore, making a good choice between parallel and series connections in a specific condition can increase the output power and the operational excitation range. The proposed interface circuit in this paper is able to check the condition in (17) periodically and connect the two PTs in parallel if the condition is satisfied; otherwise, in series. The expected output power of the proposed circuit is shown in dash curves.

According to (8), (15) and (16), the output power while using the proposed circuit can be expressed as:

$$P = f_P C_S((V_S + \Delta V_S)^2 - V_S^2) \quad \text{where}$$

$$\Delta V_S = \begin{cases} \frac{C_P}{C_S}(V_{pp(open)} - 2(V_S + 2V_D)) \\ \quad \text{if } V_{pp(open)} \geq 3(V_S + 2V_D) \\ \frac{C_P}{C_S}(\frac{V_{pp(open)}}{2} - \frac{V_S + 2V_D}{2}) \\ \quad \text{if } (V_S + 2V_D) \leq V_{pp(open)} < 3(V_S + 2V_D) \\ 0 \\ \quad \text{if } V_{pp(open)} < (V_S + 2V_D) \end{cases} \tag{18}$$

If both the two variables $V_{pp(open)}$ and V_S are swept $0\,\mathrm{V} \rightarrow 12\,\mathrm{V}$ and $0\,\mathrm{V} \rightarrow 6\,\mathrm{V}$ respectively, a three dimensional surface plot of output power can be plotted, which is shown in Fig. 7. Planes of $V_S = 2\,\mathrm{V}$ (corresponding to Fig. 6a) and $V_{pp(open)} = 12\,\mathrm{V}$ (corresponding to Fig. 6b) are highlighted in this figure. It can be seen that higher V_S requires higher $V_{pp(open)}$ to start transferring energy to the storage capacitor. With a fixed V_S, the series model is able to output much higher power than the parallel model in low excitation levels. While $V_{pp(open)}$ goes higher, this difference becomes smaller but two peak power points allows a high output power in a wide range of V_S.

III. Proposed Interface Circuit

Fig. 8 shows the implementation of the proposed interface circuit between two PTs (a bimorph cantilever is used in this implementation) and a full-bridge rectifier. An off-chip voltage regulator is employed to provide a stable power supply $V_{DD} = 1.5\,\mathrm{V}$ to power the interface circuit itself and any possible future load electronics. The two PTs are the two piezoelectric layers on a bimorph cantilever, so that they have the same frequencies, amplitudes and phases. The system architecture of the proposed circuit is also shown in the figure, which consists of a connection switching block, a power management

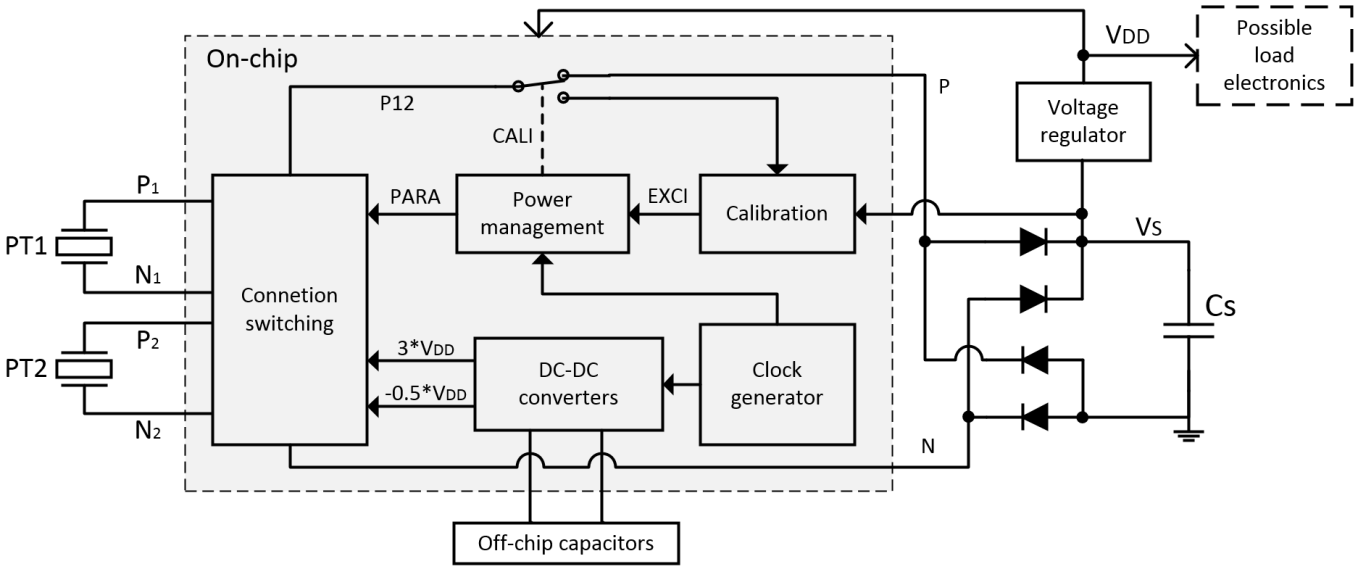


Fig. 8: Architecture of proposed system

block, a calibration block, an internal clock generator and switched-capacitor (SC) DC-DC converters. The connection switching block enables parallel or series configurations of the PTs according to the signal $PARA$ (high for parallel and low for series). The power management block is a digital block that sets the system in the "sleep mode" for most of the time and in "calibration mode" to evaluate excitation amplitudes and re-connect the two PTs. The calibration block performs the algorithm to check the condition in (17) and generates $EXCI$ pulses if the condition is satisfied. The signal $EXCI$ (short for 'excitation') indicates that the environmental excitation is high enough to make the circuit choosing parallel connection. The DC-DC converters aim to generate a high voltage level and a negative voltage level to overdrive the gates of analog switches in the connection switching block.

While the system is in "sleep mode", the calibration block is powered OFF to minimize the overall power consumption. The duration of the "sleep mode" is controlled by a digital counter in the "power management block" driven by an internally generated clock signal. This counting time can be externally set. While the "sleep mode" ends, the system goes into "calibration mode". In this mode, the connection is forced to be parallel with a high $PARA$ signal and the node P_{12} is disconnected from the node P by signal $CALI$ (short for 'calibration'); because the value $V_{pp(open)}$ in (17) requires that the two PTs are connected in parallel and in an open-circuit (not connected to the diodes). In this mode, the voltage at node P_{12} and the voltage V_S are used for comparison in an algorithm corresponding to the condition in (17). If the excitation level is high to satisfy the condition, $EXCI$ pulses will be generated to the power management block, which gives a final decision on the signal $PARA$ and the "calibration mode" finishes.

IV. Circuit Implementations

This section describes the circuit implementations of the proposed connection auto-switching interface circuit as a CMOS circuit. Some key blocks shown in Fig. 8 are presented in this section with circuit diagrams and relevant calculations.

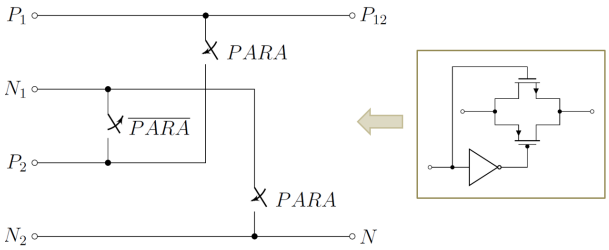


Fig. 9: Parallel-series connection switching circuitry with CMOS analogue switches

A. Parallel-series connection switching block

The parallel-series connection switching circuitry utilizes three CMOS switches, as shown in Fig. 9. The nodes P_1, N_1, P_2 and N_2 are the electrodes of the two PTs. The node N is one of the inputs of full-bridge rectifier. The node P_{12} is connected to the other input of the rectifier while the system is in "sleep mode" and to the calibration block in "calibration mode", as shown in Fig. 8. In order to make sure that the switches are fully switched ON and OFF for relevant $PARA$ signals, the gate driving voltage of $PARA$ should fully cover the voltage ranges of all the six nodes in the figure. According to Fig. 1, the voltages of V_P and V_N are between $-V_D$ and $V_S + V_D$. Hence, the low level of signal $PARA$ should be lower than $-V_D$ and its high level should be higher than $V_S + V_D$. In this implementation, voltage levels of $V_{sub} = -0.75\,\mathrm{V}$ and $V_{DDA} = 4.5\,\mathrm{V}$ are chosen to drive the switches. The N-channel MOSFETs used in the switches are isolated high-voltage transistors with a negative bulk voltage V_{sub} and the bulk voltage of the P-channel MOSFETs is V_{DDA}.

As the signal $PARA$ is generated from the power management block, which is a digital block, the voltage levels of

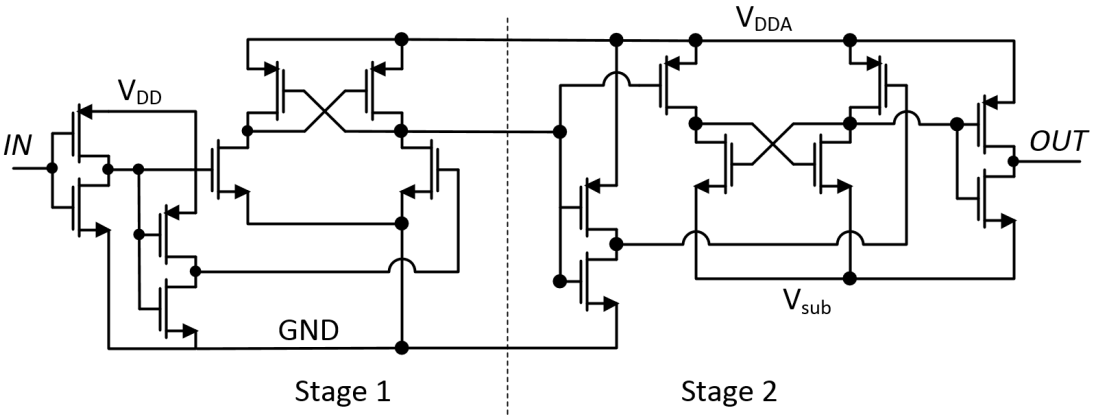


Fig. 10: Two-stage level-up shifter

$PARA$ are GND and V_{DD}, where $V_{DD} = 1.5\,\mathrm{V}$ is used in this implementation. Hence, before the signal $PARA$ from the power management block can be used to drive the switches, a level-up shifter is needed to shift the voltage level $0\,\mathrm{V}$ to $-0.75\,\mathrm{V}$ and $1.5\,\mathrm{V}$ to $4.5\,\mathrm{V}$. The reason for choosing $-0.75\,\mathrm{V}$ and $4.5\,\mathrm{V}$ as the most negative and positive voltage levels in the circuit is due to the maximum allowed voltages for the selected transistors in the HV CMOS process used in this implementation. The absolute maximum allowed voltages V_{GS} and V_{DS} for these transistors are $5.5\,\mathrm{V}$ and the oxide breakdown voltage is $7\,\mathrm{V}$. Hence, choosing $-0.75\,\mathrm{V}$ and $4.5\,\mathrm{V}$ voltage levels makes a maximum $5.25\,\mathrm{V}$ voltage difference, which makes sure all the transistors operating safely. Fig. 10 shows a two-stage level-up shifter to shift the high level of the input signal to a higher voltage and the low level to a lower voltage. The different voltage levels shown in the figure are $GND = 0\,\mathrm{V}$, $V_{DD} = 1.5\,\mathrm{V}$, $V_{DDA} = 4.5\,\mathrm{V}$ and $V_{sub} = -0.75\,\mathrm{V}$. The first stage employs a cross-coupled PMOS load and it aims to shift logic voltage levels from [$0\,\mathrm{V}$, $1.5\,\mathrm{V}$] to [$0\,\mathrm{V}$, $4.5\,\mathrm{V}$]. The second stage employs a cross-coupled NMOS load to further shift logic levels from [$0\,\mathrm{V}$, $4.5\,\mathrm{V}$] to [$-0.75\,\mathrm{V}$, $4.5\,\mathrm{V}$]. The typical quiescent current at room temperature for supply V_{DDA} is around $80\,\mathrm{pA}$ and for supply V_{DD} is around $10\,\mathrm{pA}$, so the typical total quiescent power consumption of this level-up shifter is around $0.5\,\mathrm{nW}$. Considering the process and temperature variations by using Monte-Carlo simulations, the maximum quiescent power consumption can go up to $7.3\,\mathrm{nW}$ at $150\,^{\circ}\mathrm{C}$. However, this high temperature will unlikely happen in most implementations except for specific high-temperature purposes. Besides the static power loss, the total power consumption of a shifter should also include dynamic power loss, which depends on input signal frequency and gate capacitance of switches being driven. The total power consumed by all the level shifters employed in the system will be listed in a power consumption breakdown table in Section V.

In order to provide gate overdriving voltages V_{DDA} and V_{sub}, switched capacitor (SC) DC-DC converters are employed. Fig. 11 shows the circuit diagrams of the two DC-DC converters. These two DC-DC converters perform voltage conversions with ratios $\frac{3}{1}$ and $-\frac{1}{2}$ respectively. Due to the limited chip design area reserved for this circuit, the capacitors used in the converters are off-chip SMD capacitors with $C_1 = C_2 = 1\,\mathrm{nF}$. Hence, there are totally 7 off-chip $1\,\mathrm{nF}$ capacitors employed for the DC-DC converters in this implementation. However, simulations show that the total quiescent current flowing through V_{DDA} and V_{sub} for the whole circuit is $0.3\,\mathrm{nA}$ and the total average dynamic current is $2\,\mathrm{nA}$, which make capacitors of $C_1 = C_2 = 50\,\mathrm{pF}$ sufficient to provide the required driving ability. Capacitors with these values can be readily designed on-chip to make the proposed interface circuit fully integrated.

The voltage converters are driven by two non-overlapping complementary clock signals, ϕ_1 and ϕ_2, which are generated from a single clock signal by cross-coupling the clock and its inverted version with two NOR gates and two weak inverters. Before ϕ_1 and ϕ_2 can be used to drive the converters, their levels need to be shifted through level shifters. In this implementation, the clock signal is generated by an internal on-chip ring oscillator, as shown in Fig. 12. The ring oscillator generates a raw clock signal at around $16\,\mathrm{kHz}$; this clock is then divided by 16 to drive the DC-DC converters and further divided by 16 (to $62\,\mathrm{Hz}$) to drive the power management block. In order to supply the gate-overdriving voltage levels to make sure the parallel and series configurations are firmly held, the ring oscillator and SC converters are kept powered ON. Simulations show that the ring oscillator consumes an average power of $260\,\mathrm{nW}$ and the voltage tripler and voltage half-inverter (in Fig. 11) consume $9\,\mathrm{nW}$ and $4\,\mathrm{nW}$ respectively with open outputs. Besides employing SC DC-DC converters, there are many other techniques to provide the switch gate-overdriving voltage levels, such as selecting the highest available voltage in the circuit nodes using a higher supply (HS) circuit for V_{DDA} and using a negative voltage converter (NVC) for V_{sub}, which are presented in [22]. As ring oscillators are normally power hungry and the low frequency ring oscillator employed in this paper consumes $260\,\mathrm{nW}$ power (SC converters consumes $13\,\mathrm{nW}$ extra power), using HS and NVC circuits can decrease this power consumption to $96\,\mathrm{nW}$ (calculated according to [22]). However, the circuit in this paper requires a clock signal to drive the power management block presented in section IV-C in order to periodically put the system in sleep mode,

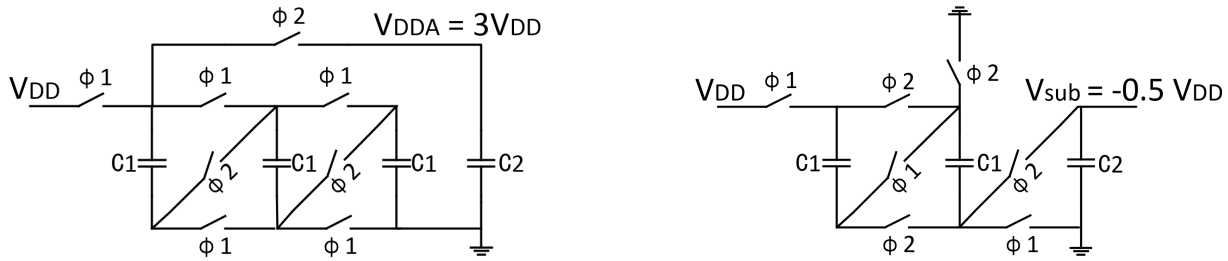


Fig. 11: Switched-capacitor (SC) converters used to generate gate overdriving voltage levels: (a) $V_{DD} \rightarrow 3V_{DD}$, (b) $V_{DD} \rightarrow -0.5V_{DD}$

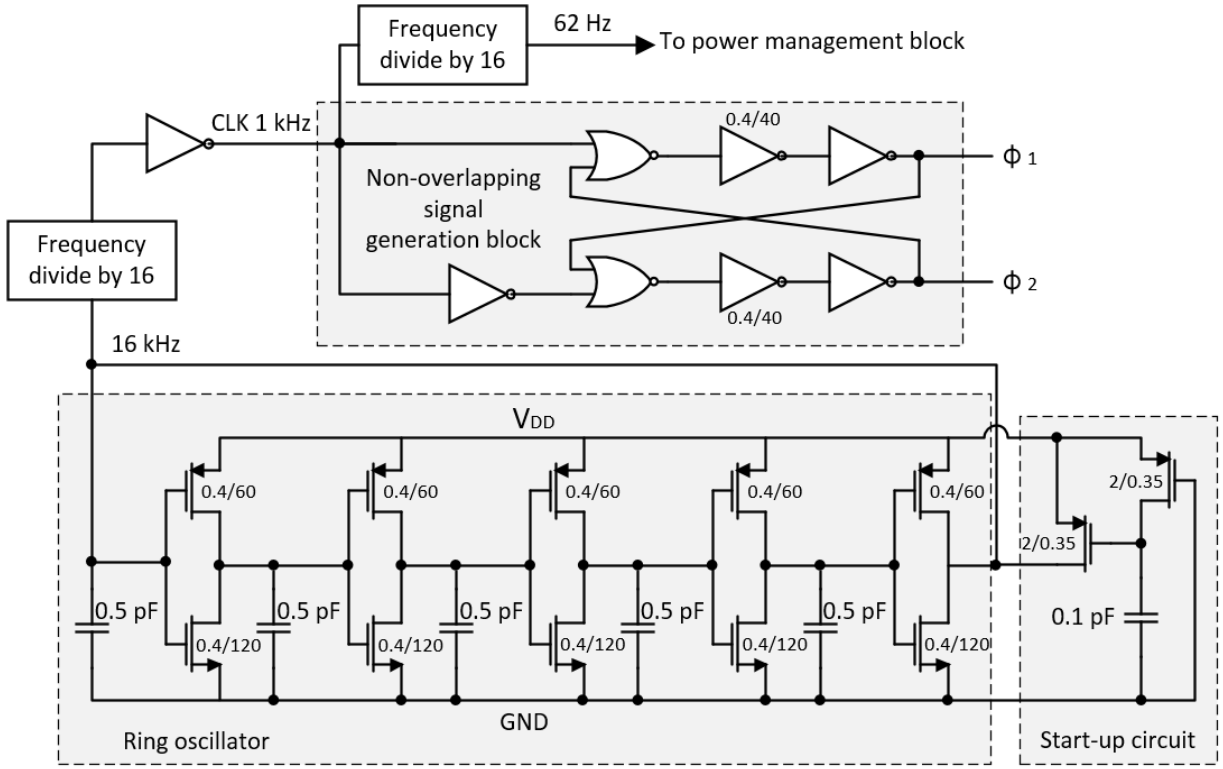


Fig. 12: Nano-power ring oscillator to provide digital clock for the SC converters and power management block, including the start-up circuitry and the non-overlapping signal generation block

and it cannot be guaranteed that the future load electronics can provide a such clock signal. As designing a ring oscillator is necessary in this implementation, SC DC-DC converters only consume $13\,\mathrm{nW}$ extra power while the HS and NVC circuits would consume more.

B. Calibration block

In the calibration state, the two harvesters are forced to be connected in parallel, so $P1$ and $P2$ are connected to $P12$; $N1$ and $N2$ are connected to N. For calibrating, $P12$ is disconnected form P, so the PTs are in an open-circuit. As $N1$ is still connected to N, the voltage at node $N1$ equals to $-V_D$ due to the diode voltage drop between the ground reference and node $N1$. Therefore, the peak-to-peak open-loop voltage between nodes $P12$ and N is now $V_{pp(open)} = 2(V_{P12} + V_D)$ (as $V_{pp(open)} = (V_{P12} - V_N)_{max} - (V_N - V_{P12})_{max} = 2(V_{P12} - V_N)_{max} = 2(V_{P12} + V_D)$). Replacing the term in (17), it becomes:

$$\begin{aligned} V_{pp(open)} &> 3(V_S + 2V_D) \\ 2(V_{P12} + V_D) &> 3(V_S + 2V_D) \\ 2V_{P12} &> 3V_S + 4V_D \\ 2(V_{P12} - 2V_D) &> 3V_S \\ \frac{1}{5}(V_{P12} - 2V_D) &> \frac{3}{10}V_S \end{aligned} \tag{19}$$

Fractions on both sides of the inequality are to make sure that the values on the two sides are in the operational range of the comparator. Fig. 13 shows the circuit diagram of calibration block to perform the comparison of (19). The

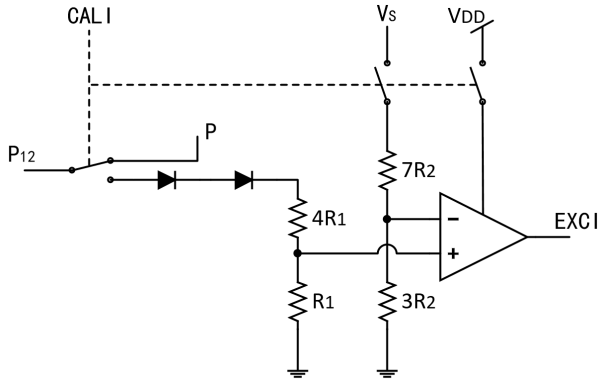


Fig. 13: Circuit diagram of the calibration block

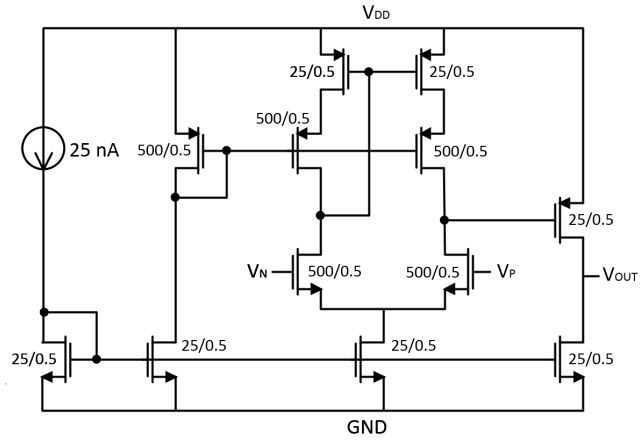


Fig. 14: Continuous time comparator to evaluate the input excitation level

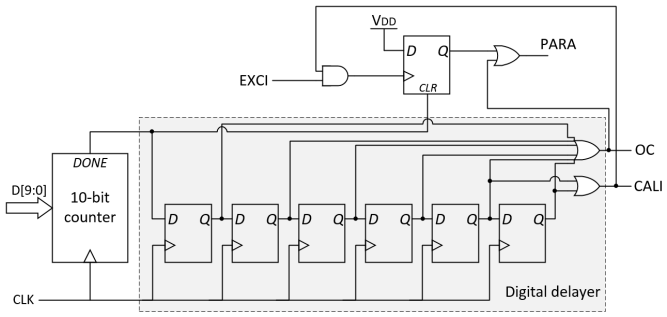


Fig. 15: Power management and parallel-series determining circuitry

two diodes used in the circuitry are the same as the ones used in the full-bridge rectifier in order to make sure they have same V_D. From this circuitry, the non-inverting input of the comparator is $\frac{1}{5}(V_{P1} - 2V_D)$ and the inverting input is $\frac{3}{10}V_S$. The unit resistances R_1 and R_2 in the circuit are set to $0.6\,\mathrm{M\Omega}$ and $0.5\,\mathrm{M\Omega}$ respectively, hence the total resistances for each of the two resistive paths are $3\,\mathrm{M\Omega}$ and $5\,\mathrm{M\Omega}$. The resistors are on-chip implemented. The current on these two branches depends on the voltage at node P_{12} and the voltage V_S. During the calibration mode while P_{12} is disconnected from the full-bridge rectifier, the voltage on the R_1 branch approximately equals to the open-circuit voltage of the PT, which can have an amplitude varying from $0\,\mathrm{V}$ to $12\,\mathrm{V}$. Choosing the middle value $6\,\mathrm{V}$ for estimation, the power loss due to this path is $3\,\mu\mathrm{W}$ (V_{P12} is a sine signal between $0\,\mathrm{V}$ and $6\,\mathrm{V}$). In terms of the R_2 branch, the V_S usually varies from $2\,\mathrm{V}$ to $6\,\mathrm{V}$; hence the average power loss due to this path is $3.2\,\mu\mathrm{W}$ (taking $V_S = 4\,\mathrm{V}$). As the two branches are cut from P_{12} and V_S in sleep mode, which takes a very majority of time, the total average power loss on these two branches equals $6.2\,\mu\mathrm{W} \times d_{cali}$, where d_{cali} represents the duty ratio of the calibration mode. The base power loss $6.2\,\mu\mathrm{W}$ for these two resistive branches can be further reduced by increasing the resistances or using off-chip resistors to provide much higher resistances. Although larger value resistors are able to reduce the base power loss to less than $1\,\mu\mathrm{W}$, they can take up additional area, either on the chip or on the test board with off-chip resistors. The resistance R_2 can be increased to a much higher value as the variation of V_S is slow. However, the value of R_1 should be below a reasonable limit because the frequency of V_{P12} signal can be quite high and the input transistors of the comparator have large sizes (500/0.5). Hence, high R_1 along with the large input capacitance of the comparator form a passive RC low-pass filter which filters out high frequency V_{P12} signal.

The output signal of this block, $EXCI$, indicates that the environmental excitation is high enough to satisfy the condition in (19). For generating the $EXCI$ signal, a continuous-time comparator is employed [23], which is shown in figure 14. A trade-off between the power loss and the performance determines the biasing current. With a $25\,\mathrm{nA}$ biasing current, the settling time of the comparator is around $40\,\mu\mathrm{s}$, which is acceptable for most of PTs as it is much shorter than the periods of PTs and the static power loss is decreased to $150\,\mathrm{nW}$. In addition, the comparator is powered OFF in the sleep mode to further decrease power loss.

C. Power management block

Fig. 15 shows a power management circuitry employed to power OFF some parts of the system for a certain time while they are not in use and to generate digital control signals. As shown in the figure, the power management circuit utilizes a 10-bit digital counter for determining the duration of sleep mode. The clock signal of this 10-bit counter is of around $62\,\mathrm{Hz}$. The 10-bit counting number D[9:0] of the counter is set externally and the system goes into "calibration mode" once it counts to the preset value D[9:0]. For instance, if D[9:0] = 255, the counter will be reset after 255 cycles of CLK, which is approximately 4 seconds. The maximum value can be set to 1023, or 16 seconds. Once the counter finishes counting, a pulse $DONE$ is generated and the counter is synchronously reset to restart counting from 0. In order to make the power management block working as expected to let system go into the two different modes alternatively for reasonable durations, the four LSBs D[3:0] are internally set to 4'b1111 and cannot be configured.

After the counter, a digital delayer using six simple D-flip-flops is employed. When the counter finishes counting,

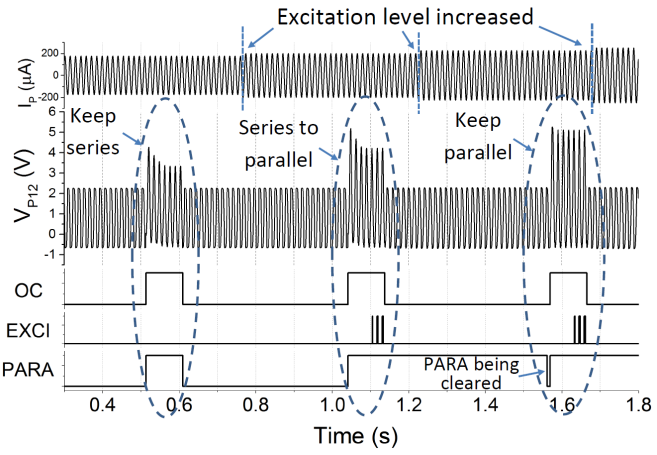


Fig. 16: Simulation results of the proposed circuit

a pulse of $DONE$ generates a pulse of OC (short for 'open-circuit') lasting for 6 clock periods and a pulse of $CALI$ (short for 'calibration') lasting for 2 clock periods. If the input of the counter is set to the maximum value D[9:0] = 1023, the calibration mode only takes $6/1024 \approx 0.6\%$ of the total time, which means the average power consumption and current leakage associated to the calibration mode are largely reduced to 0.6%. The pulse OC is used to set the prerequisite conditions for performing the algorithm in the calibration block: forcing the two PTs to be connected in parallel and in an open-circuit. During the pulse of OC, the calibration block is powered ON but its output $EXCI$ is disabled until the pulse $CALI$ is present (the last two period of the pulse OC). Because suddenly putting the PTs in open-circuit from a closed circuit may cause issues on the reference voltage, which can make the voltage at the node P_{12} going to an unexpected voltage level and the voltage at node N does not equal to $-V_D$. This is because before an OC pulse, node P_{12} is connected to one electrode of the storage capacitor C_S through a diode and node N (the other electrode of PTs) is connected to the other electrode of C_S through a another diode (refer to Fig. 8). In this case, the two diodes connect P_{12}, N and C_S and form a closed loop. As there is current flowing in this loop when energy is transferred to C_S, N should be equal to $-V_D$ (assuming N is the lower potential node). Once P_{12} is disconnected from the diode connected to C_S, there is no closed loop between P_{12} and N nodes. Although N is connected to the ground through a diode, there is no current flowing through the diode to ensure that the potential at N is $-V_D$. In this case, the voltage potential at N is not stable and it equals to the ground (0 V) at the instant of OC goes high. This introduces an V_D offset to the voltage at P_{12} because the inequality derived in (19) requires the voltage at N is $-V_D$. In order to make V_N be able to attain $-V_D$ while $V_{P(12)}$ goes high, some time is needed after OC goes high to let the diode between N and the ground "slowly" set $V_N = -V_D$. In this implementation, four periods of CLK is given. In the following two periods of CLK, $CALI$ pulse is generated which enables $EXCI$.

Fig. 16 shows the simulated waveforms of the proposed circuit. The signal I_P at the top represents the excitation amplitude, in unit of μA, which is increased gradually. The second signal V_{P12} is the voltage at the node $P12$ shown in Fig. 13. From the figure, the calibration mode is entered three times, where OC is high, in this simulation. When OC is high, the PTs are in open circuit and V_{P12} exceeds the limit $V_S + V_D$. It can be seen that V_{P12} needs a little time to stabilize before the signal $EXCI$ is enabled and can be generated at the end of the calibration state. During the first calibration mode, although the signal $PARA$ is forced to high to evaluate the excitation level, it goes low again after the calibration mode as the $EXCI$ pulse is not generated due to low excitation amplitude. After this calibration mode, I_P is increased. During the second calibration mode, it can be seen that three pulses of $EXCI$ is generated because the circuit chooses a parallel connection according to the excitation input. It is worth mentioning that the $EXCI$ pulses are generated according to the amplitude of V_{P12}, which has a frequency of 82 Hz. As mentioned before, the $EXCI$ signal is only enabled for two CLK cycles and the frequency of CLK is 62 Hz. This explains why three $EXCI$ pulses are generated in two CLK cycles. If the excitation frequency goes higher (or lower), there will be more (or less) $EXCI$ pulses generated in two CLK cycles if the amplitude is high enough. If the excitation frequency is less than 31 Hz (half frequency of CLK) such that the period of the excitation is longer than two CLK cycles, an excitation peak cannot always be observed in the two CLK cycles. Hence, $EXCI$ pulses cannot always be generated in this case. This may occasionally result in an unexpected series connection while the parallel connection is preferred under high excitation levels. Therefore, the proposed system requires the excitation frequency higher than 31 Hz to ensure correct connection switching. Before the third OC pulse, the excitation level is further increased and the PTs are expected to be connected in parallel. Right before the third OC pulse, $PARA$ goes low for one clock cycle and it goes back to high level. This is because the top single D-flip-flop in Fig. 15 is reset first before each calibration mode, which allows $PARA$ to be cleared to low level before it is forced to go high by OC signal.

The single D-flip-flop in this block is used to provide a decision on the connection type based on the signal $EXCI$, which is generated in the calibration block in Fig. 13. While the counter finishes counting, the signal $DONE$ resets the flip-flop to a low level regardless the previous connection type (parallel or series). The $CALI$ pulse is used to enable the $EXCI$ signal. If one or more $EXCI$ pulses are present in the calibration mode during the pulse of $CALI$, the output of the flip-flop goes high and keeps the two PTs connected in parallel after the calibration state. If the excitation is too low to generate a pulse of $EXCI$, $PARA$ signal will go back to low level after the calibration mode ends. An external one-time reset is performed on all of the flip-flops once the circuit is implemented and powered ON. During the simulation shown in Fig. 16, the input of the counter is set to D[9:0] = 32. This value is very small and is very impractical because the calibration mode takes a large percentage of the time (duty ratio is around $6/32 \approx 18.7\%$). During this mode, some extra

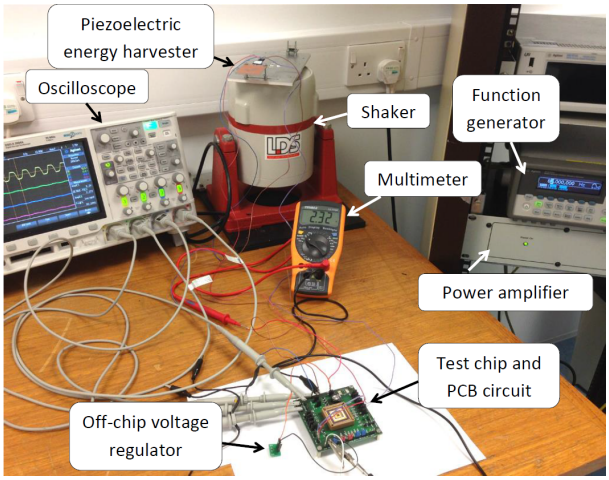


Fig. 17: Experimental setup

energy is consumed and no energy can be transferred from the PT to the storage capacitor due to the open circuit of the PT. However, this small value chosen here is to clearly show the working principle of the proposed interface circuit and to decrease the simulation time due to the slow simulation speed. As discussed above, if the maximum value D[9:0] = 1023 is chosen for the counter, the duty ratio of the calibration mode is only 0.6%.

As discussed above, a smaller calibration duty ratio results in lower power consumption but the system also reacts slowly to variations in environmental excitation. Hence, there exists a trade-off between power consumption and circuit response time. The general principle is to keep the calibration duty ratio as small as possible while the circuit is able to react to the environmental excitation amplitude variation. As the four LSBs of the input signal D[3:0] for the counter are internally set to 4'b1111, the shortest sleep time is around $0.25\,\mathrm{s}$ with a 37% calibration duty ratio. Hence, the proposed system cannot react to significant variation in excitation level faster than this value. However, the shortest sleep time preset by the circuit is impractical due to the large calibration duty ratio. Therefore, the proposed system is not suitable in environments with uncertain base vibration without target periods of time when the excitation level is high.

V. Measurement Results and Discussions

The proposed connection auto-switching interface circuit was experimentally evaluated (see Fig. 17) using a commercially available bimorph cantilevered piezoelectric harvester with dimension $47\,\mathrm{mm} \times 36\,\mathrm{mm}$ (Mide Technology Corporation V20W). A shaker (LDS V406 M4-CE) was excited at the natural frequency of the cantilever at $82\,\mathrm{Hz}$ and driven by a sine wave from a function generator (Agilent Technologies 33250A $80\,\mathrm{MHz}$ waveform generator) amplified by a power amplifier (LDS PA100E Power Amplifier). The test chip was powered by an external power supply at $1.5\,\mathrm{V}$ (can go up to $1.8\,\mathrm{V}$ for higher V_S) and an off-chip voltage regulator (ON Semiconductor NCP4681DSQ15T1G) with ultra-low ground leakage current ($I_{GND} \approx 1.5\,\mu\mathrm{A}$) is also available to allow

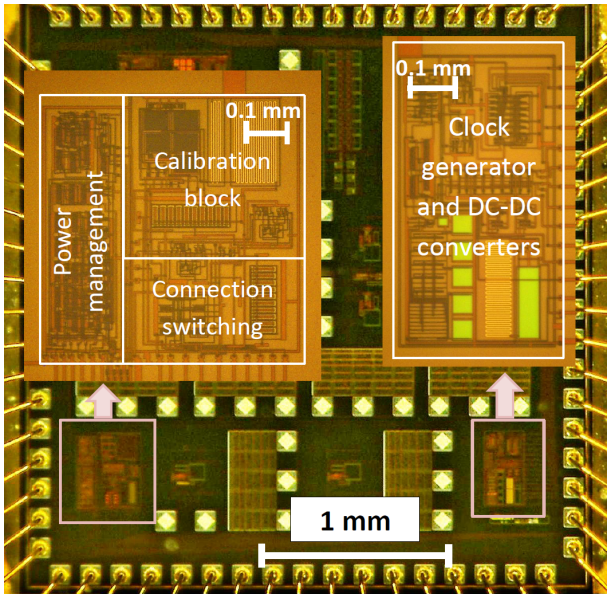


Fig. 18: Micrograph of the test chip fabricated in a $0.35\,\mu\mathrm{m}$ CMOS foundry process. The overall die size is $2.8\,\mathrm{mm} \times 3.2\,\mathrm{mm}$. The active area for the proposed circuit is around $0.5\,\mathrm{mm}^2$ excluding the pads and the remaining die area is occupied by circuits of other projects

TABLE I: Breakdown of the chip power loss and other power loss sources with simulated and measured results

Loss mechanism	Power loss	Percentage
Ring oscillator	260 nW	57.5%
DC converters	13 nW	2.9%
Level shifters	25.7 nW	5.7%
Power management	0.6 nW	0.1%
Switching block	0.3 nW	0.1%
Calibration block *	152.4 nW	33.7%
Total (circuit)	452 nW	100%
Measured circuit loss	$\sim 0.5\,\mu\mathrm{W}$	
C_S leakage	$\sim 0.24\,\mu\mathrm{W}$	

(* depends on the calibration duty ratio)

for the system to be self-powered. The components on the PCB board include a storage super capacitor (AVX BestCap BZ05CA103ZSB, measured capacitance $C_S \approx 5.2\,\mathrm{mF}$), a few $1\,\mathrm{nF}$ SMD capacitors for SC DC-DC converters, external digital inputs and pins for observing some key signals.

The proposed chip was implemented in a $0.35\,\mu\mathrm{m}$ CMOS process. Fig. 18 shows the die photo of the test chip. The active area of the proposed connection auto-switching circuit together with the DC-DC converters and the clock generator is around $0.5\,\mathrm{mm}^2$. The micrograph of the chip identifies the area occupied by the clock generator, DC-DC converters, power management block, calibration block and connection switching block.

Table I lists the simulated power loss due to different parts of the energy harvesting system. The values for the individual circuit blocks are simulated results. In terms of the power loss due to the calibration block, the duty ratio of

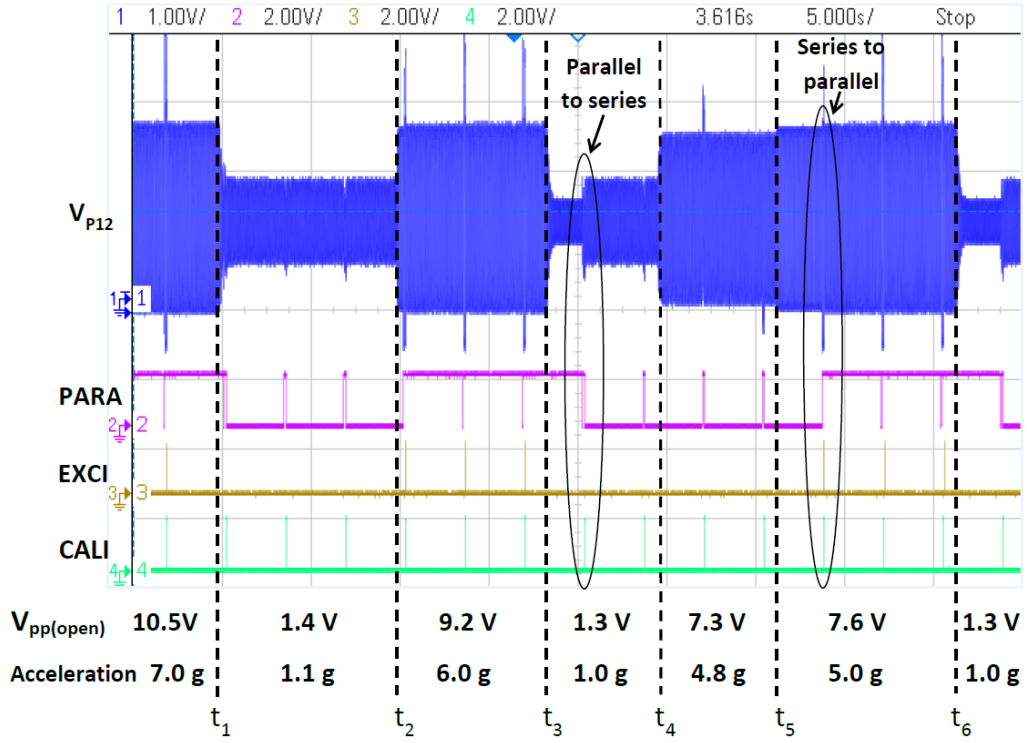


Fig. 19: Measured waveforms of signal V_{P12}, $PARA$, $EXCI$ and $CALI$ in a period of $50\,\mathrm{s}$

calibration mode during the measurement is chosen at 2.4%, corresponding to D[9:0] = 256 for the digital counter in the power management block. With a $62\,\mathrm{Hz}$ clock, the calibration mode is expected to be entered every $4\,\mathrm{s}$ and this can be observed from Fig. 19. Hence the effective power loss due to this block is $6.35\,\mu\mathrm{W} \times 2.4\% = 152.4\,\mathrm{nW}$. The simulated total power consumption of the interface circuit with a 2.4% calibration mode duty ration is $452\,\mathrm{nW}$, which is smaller than the measured value $500\,\mathrm{nW}$. This is possibly due to the excitation level and the voltage across the storage capacitor C_S during the measurements are relatively high, which increase the power loss due to the resistive branches in the calibration block as shown in Fig. 13. The storage capacitor C_S is an off-chip super capacitor of $5.2\,\mathrm{mF}$ and the power loss due to its internal leakage has been experimentally evaluated. The measurement was started by charging C_S to $4.21\,\mathrm{V}$. After 1 day 19 hours and 7 minutes of leaving it disconnected from any electronic devices, the voltage decreased to $1.86\,\mathrm{V}$ and the power loss is calculated by dividing the energy loss in the capacitor over the time. As the leakage current of C_S depends on the voltage across it, the measured power loss [$0.24\,\mu\mathrm{W}$] should be regarded as an average value for V_S between $1.86\,\mathrm{V}$ and $4.21\,\mathrm{V}$.

Fig. 19 shows measured waveforms from an oscilloscope of four signals: V_{P12}, $PARA$, $EXCI$ and $CALI$ (from top to bottom). The signals were measured in a period of $50\,\mathrm{s}$ by changing the input excitation amplitude. The signal V_{P12} is the voltage at the node P_{12}; the signal $PARA$ indicates the connection type that is being used; the signal $EXCI$ is the output signal from the calibration block indicating that the condition in (17) is satisfied and the signal $CALI$ is the output signal from the power management block indicating that the system is in "calibration mode". From the $CALI$ signal, it can be seen that the "calibration mode" was entered periodically for every $4\,\mathrm{s}$ (approximately). According to the section IV-C, the "calibration mode" starts when the digital counter finishes counting. The first cycle after the counting ends, a signal $DONE$ is generated to reset a flip-flop to have a series connection (refer to Fig. 15). This explains why the signal $PARA$ goes low for a very short time (actually for one clock cycle) when "calibration mode" starts with a high level $PARA$. After the $PARA$ is reset to low level, the signal delayer in the power management block forces $PARA$ to high level for a few cycles to evaluate the excitation. This forced high $PARA$ pulses can also be seen from the Fig. 19 corresponding to pulses $CALI$. The signal $EXCI$ indicates the result after evaluating the excitation amplitude according to the algorithm in (19). If a pulse of $EXCI$ is present for a "calibration mode", the signal $PARA$ keeps high after the mode ends; otherwise, $PARA$ goes low because the excitation is too low to generated a $EXCI$ pulse.

During the $50\,\mathrm{s}$ measurement, the excitation amplitude was changed 6 times, which are marked as t_1, t_2, t_3, t_4, t_5 and t_6 in the figure. The excitation amplitudes for all the time intervals are shown at the bottom of the figure as the peak-to-peak open-circuit voltage of the PT $V_{pp(open)}$ and the corresponding acceleration level in unit of the gravity. As t_1 and t_2 are slightly before calibration states start, the effect of different connection types on the signal V_{P12} is not observable. Hence, explanations on the figure will be based on the period after t_2. From the figure, several $CALI$ pulses can be found between t_2 and t_3, where pulses of $EXCI$ are

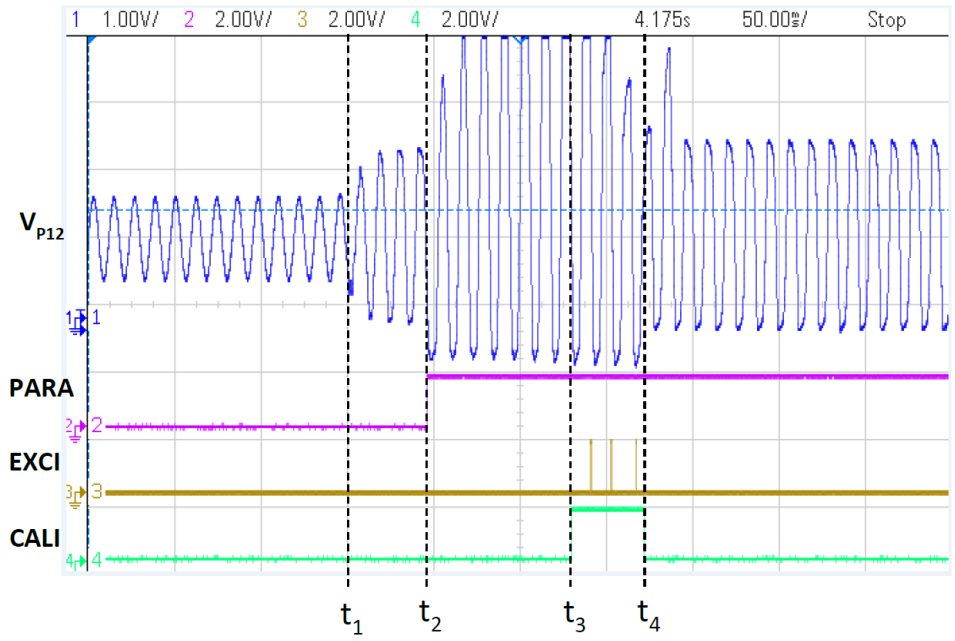


Fig. 20: Measured waveforms in $0.5\,\mathrm{s}$ while connection is being changed from series to parallel

generated. This means the excitation level is high to satisfy the condition in (19). As a result, $PARA$ keeps at high level after each calibration mode. During the calibration modes, it can be seen that spikes are present in the signal V_{P12}. This is because the PTs are disconnected from the full-bridge rectifier during the calibration mode (open-circuit), hence V_{P12} is not limited below $V_S + V_D$ and it can go higher. Similar spikes can also be observed for some of the other calibration states but spikes are not present for low excitations when V_{P12} cannot attain $V_S + V_D$. The excitation amplitude is then significantly decreased at time t_3 and a sudden drop in V_{P12} can be observed. During the calibration state after t_3 (marked in the left ellipse), no $EXCI$ pulse is present, which results in a series connection. Once the PTs are connected in series, the amplitude of signal V_{P12} can be observed to be doubled because series connection doubles the voltage across the PTs.

The excitation is then increased at time t_4 where a sudden amplitude increase of V_{P12} can be observed. However, the $EXCI$ signal still keeps low for the following two calibration states because the excitation level is not high enough. The excitation is further increased at t_5. The following calibration state confirms that the condition in (19) is satisfied and a pulse $EXCI$ is generated. As a result, the $PARA$ goes high (marked in the second ellipse).

Fig. 20 shows the waveforms of the four signals in a short period of time while the connection is being changed from series to parallel. At time t_1, the excitation is increased and the resulting V_{P12} can be observed from the figure. From time t_2 to t_4, the connection is forced to be parallel and $PARA$ goes high. During this time, the PTs are in an open-circuit hence V_{P12} can go very high. Between t_2 and t_3, the excitation evaluation is not enabled because a little time is needed to let V_{P12} become stable (detailed explanations are in section IV-C). Between t_3 and t_4, the signal $CALI$ goes high to

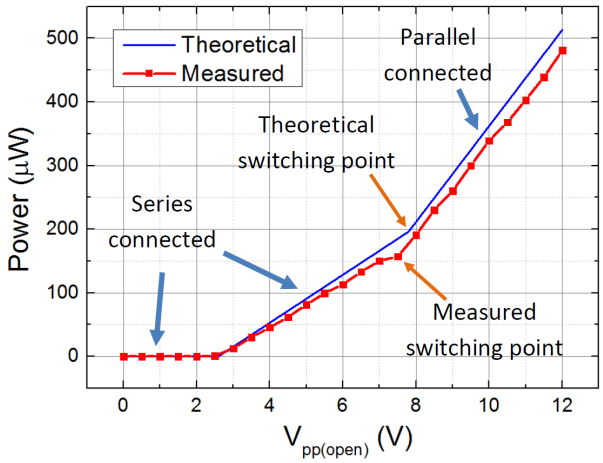
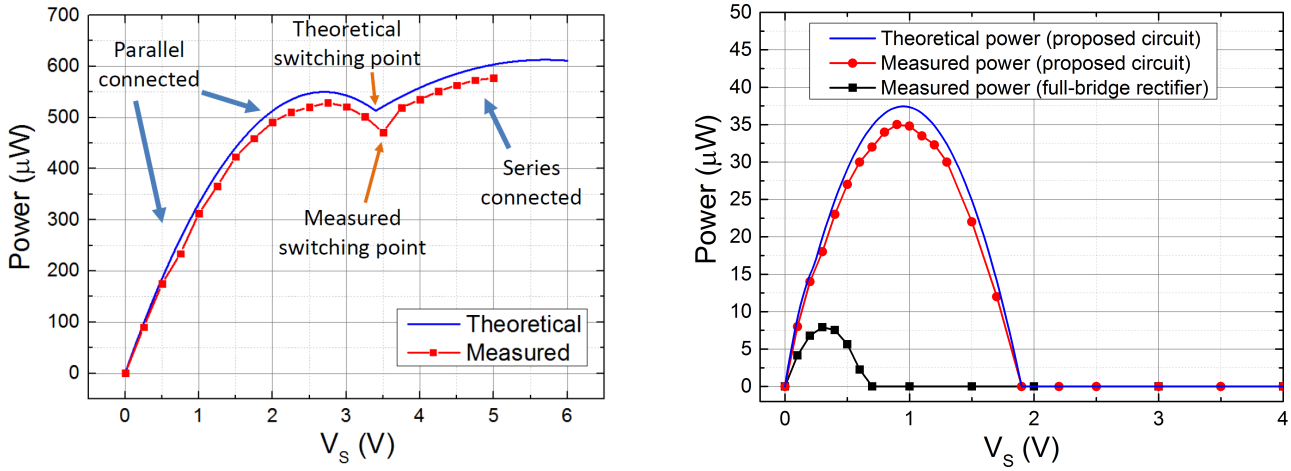


Fig. 21: Output power comparison between theoretical and measured results as a function of excitation level with fixed $V_S = 2\,\mathrm{V}$ (diode voltage drop $V_D = 0.3\,\mathrm{V}$)

enable the $EXCI$ signal; therefore, three $EXCI$ pulses are generated due to satisfying the condition in (19). These pulses indicate that the connection will be parallel after the calibration state; hence, $PARA$ keeps high after t_4.

In order to measure the output electrical power transferred to the storage capacitor C_S at a given $V_{pp(open)}$ and V_S, the voltage increase in C_S in a short period of time is measured to calculate the energy increase in this time. The formula of calculating the output power is: $P = C_S(V^2_{S(end)} - V^2_{S(start)})/2T$, where $V_{S(start)}$ is the starting voltage of V_S, $V_{S(end)}$ is the ending voltage of V_S and T is the time used to charge C_S from $V_{S(start)}$ to $V_{S(end)}$. As V_S is increasing during measurement and the output power should be obtained at some fixed V_S values, the $V_{S(start)}$ and $V_{S(end)}$ are chosen to be close to



(a) (b)

Fig. 22: Theoretical and measured output power in function V_S using proposed circuit and full-bridge rectifier under different excitation levels. (a) With a fixed excitation level of $V_{pp(open)} = 12\,\text{V}$ (equivalent to acceleration level of $8.0\,\text{g}$); (b) $V_{pp(open)} = 2.5\,\text{V}$ (equivalent to $1.8\,\text{g}$). Diode voltage drop $V_D = 0.3\,\text{V}$

make the results accurate. While measuring the output power at $V_S = 2\,\text{V}$, for instance, $V_{S(start)}$ and $V_{S(end)}$ are chosen at $1.9\,\text{V}$ and $2.1\,\text{V}$ with a fixed excitation level $V_{pp(open)}$. The time consumed to charge C_S from $1.9\,\text{V}$ to $2.1\,\text{V}$ is recorded by a stopwatch (of a smart phone) and the output power transferred to C_S can therefore be calculated.

Fig. 21 shows the measured output power compared to theoretical results with fixed $V_S = 2\,\text{V}$ and changing excitation level, where the highest $V_{pp(open)}$ ($12\,\text{V}$) corresponds to acceleration of $8.0\,\text{g}$. As $V_S = 2\,\text{V}$ and $V_D = 0.3\,\text{V}$ are used in experiments, the expected threshold voltage for pure parallel model is $2(V_S + 2V_D) = 5.2\,\text{V}$ and the expected switching point for parallel and series connection is $3(V_S + 2V_D) = 7.8\,\text{V}$. Compared to the pure parallel model, the proposed circuit can let the rectifier start extracting energy from the PTs at a lower threshold voltage $2.6\,\text{V}$. Compared to the pure series model, the circuit extracts more energy while excitation amplitudes are higher than the switching point such that $V_{pp(open)} > 7.8\,\text{V}$. The measured results show that the switching point is shifted to near $7.5\,\text{V}$ and this is due to non-ideal diodes used in measurements. Non-ideal diodes allow forward leakage current flowing through while the forward voltage is lower than V_D; hence the effective V_D is lower than $0.3\,\text{V}$, which makes the switching point shifting leftwards on the graph.

Fig. 22 shows the measured results with the proposed circuit and a full-bridge rectifier at fixed excitation levels ($V_{pp(open)} = 12\,\text{V}$ in the left figure and $V_{pp(open)} = 2.5\,\text{V}$ in the right figure) with V_S varying from $0\,\text{V}$ to $5\,\text{V}$. The results in Fig. 22a show that the switching point is measured at $V_S = 3.5\,\text{V}$, which is slightly higher than the theoretical value $3.3\,\text{V}$. This is also due to the non-ideal diodes used in measurements. The switching point is set as $V_{pp(open)} = 3(V_S + 2V_D)$. While non-ideal diodes have lower V_D values, V_S goes higher to keep a constant $V_{pp(open)}$. This explains the difference between theoretical and measured results. At a high excitation level ($V_{pp(open)} = 12\,\text{V}$) in Fig. 22a, there exists a maximum power point for each of the two connection types. With the proposed interface circuit, the energy harvesting system is able to attain both of the two peak power points at $V_S = 2.6\,\text{V}$ and $V_S = 5.5\,\text{V}$, which enable a wide range of V_S to obtain high output power. The same experiments were performed at a low excitation level ($V_{pp(open)} = 2.5\,\text{V}$) in Fig. 22b. The results show that the output electrical power using the proposed circuit can attain a peak power of $34.9\,\mu\text{W}$, which is $4.5\times$ higher than the power obtained from a simple full-bridge rectifier, which is $7.8\,\mu\text{W}$. This is due to the series connection chosen by the circuit because the series model outputs much higher power than the parallel counterpart at low excitation levels. In addition, it can be seen that the extra power consumption introduced by the interface circuit $0.5\,\mu\text{W}$ shown in Table I is far lower than the extra power extracted by this circuit compared to using a simple full-bridge rectifier.

Fig. 23 shows the measured electrical output power while $V_{pp(open)}$ is varied from $0\,\text{V}$ to $12\,\text{V}$ with steps of $1\,\text{V}$ and V_S is varied from $0\,\text{V}$ to $5\,\text{V}$ with steps of $0.5\,\text{V}$. There are 13 $V_{pp(open)}$ values and 11 V_S values chosen, hence totally 143 output power values measured. This figure illustrates the performance of the circuit in the full ranges of excitation level and V_S. The results shown in Fig. 21 and Fig. 22 are highlighted in the $V_S = 2\,\text{V}$, $V_{pp(open)} = 12\,\text{V}$ and $V_{pp(open)} = 2.5\,\text{V}$ planes. The middle dashed curve separates the parallel and series configurations according to different values of $V_{pp(open)}$ and V_S.

Fig. 24 shows the measured power efficiency of the proposed interface circuit while an external power supply is used and it is self-powered with an off-chip voltage regulator. While the circuit is self-powered using an off-chip voltage regulator, the efficiency is reduced significantly. Although the leakage current of chosen voltage regulator is as low as $1.5\,\mu\text{A}$, the energy conversion efficiency is relatively low, which pulls down the overall efficiency. [28] presents an on-chip high-efficiency

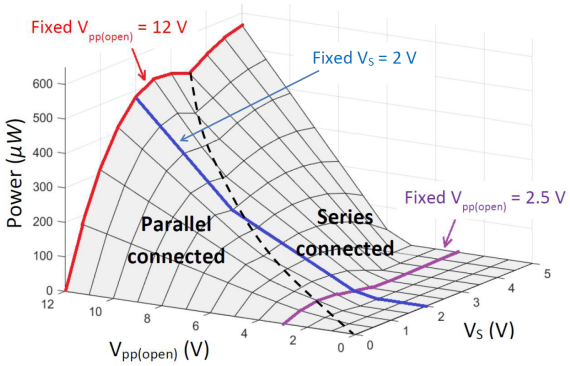


Fig. 23: 3-D surface plot of measured output power in function of $V_{pp(open)}$ and V_S

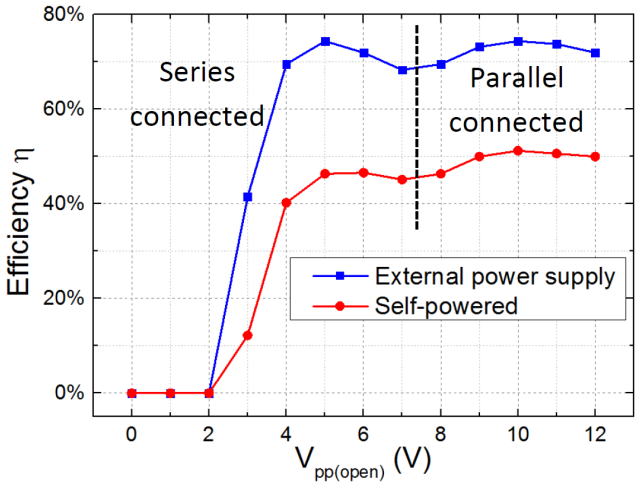


Fig. 24: Measured power efficiency of the proposed interface circuit while it is externally powered and self-powered ($V_S = 2\,\mathrm{V}$)

SC DC-DC converter with a nominal output voltage $1.5\,\mathrm{V}$ and efficiency up to 92%, which can be a very good substitute of the off-chip voltage regulator to increase the overall efficiency. However, the voltage regulator employed here is just to allow for the possibility of the proposed circuit being self-powered for an energy autonomous module. The performance of the interface circuit itself should be the highlight of this paper. From the figure, it can be clearly found that there are two peak efficiency points because the circuit is trying to configure the PTs in a better way to output higher power. While $V_{pp(open)}$ goes high from $0\,\mathrm{V}$, the power efficiency goes higher and attains its first peak near $V_{pp(open)} = 5\,\mathrm{V}$. When the excitation level keeps being increased, the efficiency decreases. When $V_{pp(open)}$ goes higher than $7\,\mathrm{V}$, the interface circuit configures the connection of the two PTs from series to parallel in order to keep the high power efficiency; therefore, the circuit is able to attain a second peak efficiency point. The dashed line in the figure shows the different connections the circuit chooses and it can be found that the first peak is due to series and the second peak is due to parallel connection. Compared to many other interface circuit, the proposed circuit enables a high power efficiency in a wide range of excitation levels.

Table II compares the performance of the proposed circuit against some reported interface circuits for piezoelectric vibration energy harvesters. Apart from the circuit presented in this paper, all of other circuits require inductors to improve performance and some may require inductors in the range of millihenries. A fully-integrated design in this paper makes a significant contribution to reducing the overall volume of the system. Although the PT employed in this implementation is relatively big compared to a SMD inductor and an inductorless design does seem to reduce the overall system volume significantly; however, using an inductorless and fully-integrated interface circuit is a very practical consideration for volume-limited MEMS piezoelectric energy harvesters [29]. All the devices needed for the proposed power management circuit are a $2.8\,\mathrm{mm} \times 3.2\,\mathrm{mm}$ chip (wire-bonder can be used instead of a chip carrier and socket), a $5.2\,\mathrm{mF}$ storage capacitor and a SC-70-5 case voltage regulator (in the case that the voltage regulator is not implemented on-chip); hence the volume is expected to be less then $0.5\,\mathrm{cm}^3$.

As discussed in section II-C and experimentally verified in this section, the proposed scheme lowers the required excitation level by 50% and always chooses the connection type outputting higher power. In real world implementations, the ambient vibration amplitude is likely to vary with time and the proposed circuit is able to detect the excitation level in order to achieve high power efficiency in a wide range of excitation amplitudes. Concerning the performance boost compared to a full-bridge rectifier, the voltage drop of diodes used in the listed publications (including this work) are different, making any fair comparison difficult to carry out. For example, the diodes used in [26] are with nearly zero voltage drop. If [26] employs the same diodes as this paper, the performance boost should have a higher value and may be even higher than the performance achieved by the circuit in this paper. However, the highlight of the proposed interface circuit is not to achieved a highest possible output power; it aims to moderately increase the performance compared to a full-bridge rectifier while addressing the three drawbacks of SSHI and SECE circuits. A sub-micro watt inductorless fully-integrated interface circuit design allows for a significant decrease in the volume in compact system designs. In addition, the proposed circuit presents a different architecture and it dynamically configures the connection of two PTs to achieve higher power efficiency over a wide range of excitation amplitudes. Furthermore, as it does not generate synchronized current pulses in the piezoelectric materials, the proposed circuit is less subject to the SSD effect even for highly coupled PTs. Therefore, the mechanical vibration of the PTs will be less affected or damped, which extends the range over which the rectifier operates efficiently.

VI. Conclusion

An adaptive sub-micro watt design for a piezoelectric energy harvesting interface circuit is proposed in this paper. The proposed circuit can be used to automatically connect two piezoelectric transducers (with same frequencies, amplitudes and phases) in parallel or in series according to the environmental excitation level and the voltage across the storage

TABLE II: Performance comparison with reported interface circuits

Publication	Techniques	Power consumption	PT	$V_{pp(open)}$	C_P	Frequency	Inductor?	Performance boost to FB
JSSC2010 [16]	Bias-flip	2 µW	Mide V22B	2.4 V	18 nF	225 Hz	Yes	4×
TIEL2012 [24]	SSHI	N.A.	T120-A4E Piezo	5.84 V	33.47 nF	30 Hz	Yes	2×
JSSC2012 [25]	PSCE	5.8 µW	Mide V22B	12.6 V	19.5 nF	174 Hz	Yes	1.23×
JSSC2014 [18]	MS-SECE	$\geq$ 1 µW	Murata	40 V	23 nF	100 Hz	Yes	N.A.
JSSC2014 [26]	Energy-investing	0.63 µW	Mide V22B	2.6 V	15 nF	143 Hz	Yes	3.6×
TPEL2015 [17]	SSHI	20 µW	Mide V22B	3.28 V	18 nF	225 Hz	Yes	4.5×
TPEL2016 [27]	SECE	0.43 µW	Q220-A4303YB	2 V	52 nF	60 Hz	Yes	3×
This work	Connection switching	0.5 µW	Mide V22W	2.5 V	115 nF	82 Hz	No	4.5×

capacitor. The theoretical output power of both parallel and series models are calculated and compared in order to find the condition to switch between the two connection types.

The proposed circuit facilitates transferring energy from the piezoelectric material to the storage capacitor at lower excitation amplitudes and it can maintain at high energy conversion efficiency over a wide range of excitation levels. This shows its strong suitability to real world vibration, where the excitation amplitude varies unpredictably. As opposed to other high-performance synchronized switch interface circuits, such as SSHI or SECE, the proposed circuit does not introduce current pulses to invert or extract charge from PTs. Hence, the performance is less affected from synchronized switch damping, especially when highly-coupled PTs are employed. Furthermore, the inductorless design enables a fully CMOS integrated implementation, which enables a reduction in overall system volume, especially for compact systems such as MEMS energy harvesters.

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